a second embedded diffusion layer formed as part of a second vertical type bipolar transistor directly on the substrate, in a second upper part of the substrate, and within a lower part of the epitaxial layer,

wherein the first embedded diffusion layer is not disposed within the second embedded diffusion layer,

wherein the second embedded diffusion layer is a second conductive type second embedded diffusion layer that is a different conductive type from the first conductive type substrate and includes an impurity concentration that is less than the impurity concentration of the first embedded diffusion layer and is equal to or higher than that of the epitaxial layer, and

wherein a peak position of an impurity concentration of the first embedded diffusion layer resides at a first distance from the datum surface of the substrate and a peak position of an impurity concentration of the second embedded diffusion layer resides at a second distance from the datum surface of the substrate such that the first distance is greater than the second distance.

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20. (Amended Three Times) A semiconductor device according to claim 1, further comprising:

a first base layer disposed between two first graft base layers and disposed above the first embedded diffusion layer on the epitaxial layer to define a first epitaxial thickness between the first base layer and the first embedded diffusion layer; and

a second base layer disposed between two second graft base layers and disposed above the second embedded diffusion layer on the epitaxial layer to define a second epitaxial thickness between the second base layer and the second embedded diffusion layer,

wherein the first epitaxial thickness is less than the second epitaxial thickness, and

wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer.

24. (Amended One Time) A semiconductor device according to claim 1, wherein the second vertical type bipolar transistor includes a base layer disposed between two graft base layers and wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer.

27. (New) A semiconductor device, comprising:

a substrate comprising a first surface that defines a datum;

a high speed diffusion layer comprising a first surface disposed above the datum at a first height;

a high voltage diffusion layer comprising a first surface disposed at a second height, wherein the second height is substantially at the datum;

a high speed base layer comprising a lower surface that faces the first surface of the high speed diffusion layer and is disposed at a first speed height from the datum;

a high voltage base layer comprising a lower surface that faces the second surface of the high voltage diffusion layer and is disposed at a first voltage height from the datum,

wherein the first speed height of the high speed base layer is equal to the first voltage height of the high voltage base layer;

an epitaxial layer, wherein the epitaxial layer is disposed between the first surface of the high speed diffusion layer and the lower surface of the high speed base layer, and wherein only the epitaxial layer is disposed between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer,

wherein the high speed (HS) diffusion layer comprises a peak impurity concentration (HSPIC) value and wherein the high voltage (HV) diffusion layer comprises a peak impurity

concentration (HVPIC) value, such that the high voltage peak impurity concentration (HVPIC) value is less than the high speed peak impurity concentration (HSPIC) value, and

wherein each impurity concentration of the high voltage diffusion layer that is located between the high voltage peak impurity concentration (HVPIC) and the datum is higher than each impurity concentration of the epitaxial layer that is located between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer.

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28. (New) The semiconductor device of claim 27,

wherein the high speed (HS) diffusion layer comprises a peak impurity concentration (HSPIC) value that is disposed at distance Y_{HSPIC} below the datum,

wherein the high voltage (HV) diffusion layer comprises a peak impurity concentration (HVPIC) value that is disposed at distance Y_{HVPIC} below the datum, and

wherein $Y_{HVPIC} > Y_{HSPIC}$.

29. (New) The semiconductor device of claim 27,

wherein the epitaxial layer between the first surface of the high speed diffusion layer and the lower surface of the high speed base layer defines a thin collector layer, wherein the epitaxial layer between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer defines a thick collector layer,

wherein the thick collector layer is thicker than the thin collector layer.